WHAT IS CLAIMED IS:

1. A microprocessor comprising:

a main memory which stores instructions;

a queue buffer which pre-fetches and stores instructions from the main memory;

a program counter which generates an address on the main memory in which an instruction to be next executed is stored;

an instruction decoder which receives and decodes instructions output from the queue buffer; and

a queue controller controls input and output of instructions to the queue buffer based on the address generated and output from said program counter,

wherein when said instruction decoder recognizes reception of a predetermined branch instruction, it processes all the instructions preceding a branch end specified by the branch instruction as an operand of the branch instruction, outputs an instruction word length of the branch instruction including the operand to the program counter thereby updating the address of the program counter, and provides a control so as not to flush the queue buffer.

2. The microprocessor according to claim 1, wherein a label is used so as to specify the branch end.

3. The microprocessor according to claim 1, wherein a relative address between the branch instruction and branch end is specified so as to specify the branch end.

4. The microprocessor according to claim 3, wherein said queue controller carries out the input and output control of instructions to the queue buffer so that a plurality of the previous instructions, which correspond to a predetermined number of relative addresses from the instruction that is currently being executed, are allowed to remain, and

a minus relative address may be specified as the relative address.

5. A microprocessor comprising:

a main memory which stores instructions;

a queue buffer which pre-fetches and stores instructions from the main memory;

a program counter which generates an address on the main memory in which an instruction to be next executed is stored;

an instruction decoder which receives and decodes

instructions output from the queue buffer; and

a queue controller controls input and output of instructions to the queue buffer based on the address generated and output from said program counter,

wherein when said instruction decoder recognizes reception of a predetermined branch instruction, it processes all the instructions preceding a branch end specified by the branch instruction as NOP instructions, outputs an instruction word length corresponding to the branch instruction and the NOP instructions to the program counter thereby updating the address of the program counter, and provides a control so as not to flush the queue buffer.